DETAILED ACTION

Response to Arguments

Applicant's arguments filed 19 March 2007 have been fully considered but they are not persuasive. The applicant argues that Takehashi does not disclose the structure of a fillet on the conductive region at the corner between the LDD region and the upstanding gate region. However, the manner in which the claim is written does not structurally nor materially define "a fillet" therefore any arbitrary element may constitute "a fillet", in which Takehashi teaches having layer (3) formed at the corner of the conductive spacer (414, 4141).

Claim Objections

Claim 9 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Independent Claim 8 recites "depositing a layer of conductive material … wherein the layer of conductive material has a thickness less than that of the gate" and dependent Claim 9 recites "depositing the layer of conductive material to a thickness which is less than that of the gate".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Takehashi et al. (PCT Publication No. WO00/54339). The English equivalent, Takehashi et al. (U.S. Patent 6,624,473 B1), is used hereinafter.

Referring to Claim 1, Takehashi teaches, in Fig. 3, a TFT comprising a polycrystalline silicon channel (170) extending between a source (150) and drain (160), a gate (4) overlying the channel, and of a thickness to define an upstanding gate sidewall, an LDD region (152, 162), and a spacer (414, 4141) overlying the LDD region (152, 162), wherein the spacer (414, 4141) comprises a conductive region that both overlies the LDD region (152, 162) and extends along the upstanding gate (4) sidewall.

Referring to Claim 2, Takehashi teaches all of the limitations of Claim 1 wherein the conductive region (414, 4141) comprises a layer that is thinner than the thickness of the gate (4) and has a first portion (4141) overlying the LDD region and a second portion (414) extending along the upstanding side wall of the gate (4).

Referring to Claim 3, Takehashi teaches all of the limitations of Claims 1 and 2 wherein the conductive region (414) comprises a layer of conductive material (metal).

Referring to Claim 4, Takehashi teaches all of the limitations of Claims 1-3 wherein the layer is a metallic layer. The language, term, or phrase "metallic layer deposited by sputtering", is directed towards the process of sputtering. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language "metallic layer deposited by sputtering" only requires the layer to be a metallic layer, which does not distinguish the invention from Takehashi, who teaches the structure as claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takehashi et al.

Referring to Claim 5, Takehashi teaches all of the limitations of Claims 1-3 but does not explicitly teach wherein the layer comprises a doped semiconductor material. However, it is notoriously well known that doped polysilicon is functionally equivalent to a metal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a doped polysilicon layer as the conductive layer instead of a metal layer as taught by Takehashi because this would allow for greater and more precise control of conductivity and resistance of the gate electrode.

Allowable Subject Matter

Claims 8 and 10-17 are allowed.

Refer to previous office action for reasons of indicating allowable subject matter.

Conclusion

(Restarting Period for Reply)

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

/Steven Loke/
Supervisory Patent Examiner, Art Unit 2818